Features:

- ✧ Hot pluggable CFP4 MSA form factor
- ✧ Compliant to IEEE 802.3ba 100GBASE-LR4 and CFP-MSA-CFP4-HW-Specification
- ✧ Transmitter: cooled 4x25Gb/s LAN WDM EML TOSA (1295.56, 1300.05, 1304.58, 1309.14nm)
- ✧ Receiver: 4x25Gb/s PIN ROSA
- ✧ 4x28G Electrical Serial Interface (CEI-28G-VSR)
- ✧ MDIO management interface with digital diagnostic monitoring
- ✧ Up to 10km reach for G.652 SMF
- ✧ Duplex LC receptacle
- ✧ Single +3.3V power supply
- ✧ Power consumption less than 5.5W
- ✧ Operating case temperature: 0~70^{o}C
- ✧ RoHS-6 compliant

Applications:

- ✧ 100GBASE-LR4 Ethernet
- ✧ OTN OTU4

General Description:

OPWAY‘s C4E10 is a 100Gb/s transceiver module for optical communication applications compliant to 100GBASE-LR4 of the IEEE P802.3ba standard. The module converts 4 input channels of 25Gb/s electrical data to 4 channels of LAN WDM optical signals and then multiplexes them into a single channel for 100Gb/s optical transmission. Reversely on the receiver side, the module de-multiplexes a 100Gb/s optical input into 4 channels of LAN WDM optical signals and then converts them to 4 output channels of electrical data.

The central wavelengths of the 4 LAN WDM channels are 1295.56, 1300.05, 1304.58 and 1309.14 nm as members of the LAN WDM wavelength grid defined in IEEE 802.3ba. The high performance cooled LAN WDM EA-DFB transmitters and high sensitivity PIN receivers provide superior performance for 100Gigabit Ethernet applications up to 10km links and compliant to optical interface with IEEE802.3ba Clause 88 100GBASE-LR4 requirements.
The product is designed with form factor, optical/electrical connection and MDIO interface according to the CFP4 Multi-Source Agreement (MSA). The innovative design has all the fibers inside the CFP4 package configured without any splicing or non-permanent connector. Also, fiber routines are neatly organized and fixed inside a stainless steel container.

1.Functional Description

This product contains a duplex LC connector for the optical interface and a 56-pin connector for the electrical interface. Figure 1 in Section 3 shows the functional block diagram of this product.

Transmitter Operation

The transceiver module receives 4 channels of 25Gb/s electrical data, which are processed by a 4-channel Clock

and Data Recovery (CDR) IC that reshapes and reduces the jitter of each electrical signal. Subsequently, each of 4 EML laser driver IC's converts one of the 4 channels of electrical signals to an optical signal that is transmitted from one of the 4 cooled EML lasers which are packaged in the Transmitter Optical Sub-Assembly (TOSA). Each laser launches the optical signal in specific wavelength specified in IEEE802.3ba 100GBASE-LR4 requirements. These 4-lane optical signals will be optically multiplexed into a single fiber by a 4-to-1 optical WDM MUX. The optical output power of each channel is maintained constant by an automatic power control (APC) circuit. The transmitter output can be turned off by TX_DIS hardware signal and/or through MDIO module management interface.

Receiver Operation

The receiver receives 4-lane LAN WDM optical signals. The optical signals are de-multiplexed by a 1-to-4 optical DEMUX and each of the resulting 4 channels of optical signals is fed into one of the 4 receivers that are packaged into the Receiver Optical Sub-Assembly (ROSA). Each receiver converts the optical signal to an electrical signal. The regenerated electrical signals are retimed and de-jittered and amplified by the RX portion of the 4-channel CDR. The retimed 4-lane output electrical signals are compliant with IEEE CAUI-4 interface requirements. In addition, each received optical signal is monitored by the DOM section. The monitored value is reported through the MDIO section. If one or more received optical signal is weaker than the threshold level, RX_LOS hardware alarm will be triggered.

MDIO Interface

The CFP4 module supports the MDIO interface specified in IEEE802.3ba Clause 45. It supports alarm, control and monitor functions via hardware pins and via an MDIO bus. Upon module initialization, these functions are available. CFP4 MDIO electrical interface consists of 6 wires including 2 wires of MDC and MDIO, as well as 3 Port Address wires, and the Global Alarm wire. MDC is the MDIO Clock line driven by host and MDIO is the bidirectional data line driven by both host and module depending upon the data directions. The CFP4 uses pins in the electrical connector to instantiate the MDIO interface as listed in Table 1. MDIO Interface Pins.

Table 1. MDIO Interface Pins

PIN	Symbol	Description	I/O	Logic	"H"	"L"
13	GLB_ALRMn	Global Alarm	O	3.3V LVCMOS	OK	Alarm
18	MDIO	Management Data Input Output Bi-Directional Data	I/O	1.2V LVCMOS		
17	MDC	MDIO Clock	I	1.2V LVCMOS		
19	PRTADR0	MDIO port address bit 0	I	1.2V LVCMOS	per MDIO document	
20	PRTADR1	MDIO port address bit 1	I	1.2V LVCMOS		
21	PRTADR2	MDIO port address bit 2	I	1.2V LVCMOS		

2.Transceiver Block Diagram

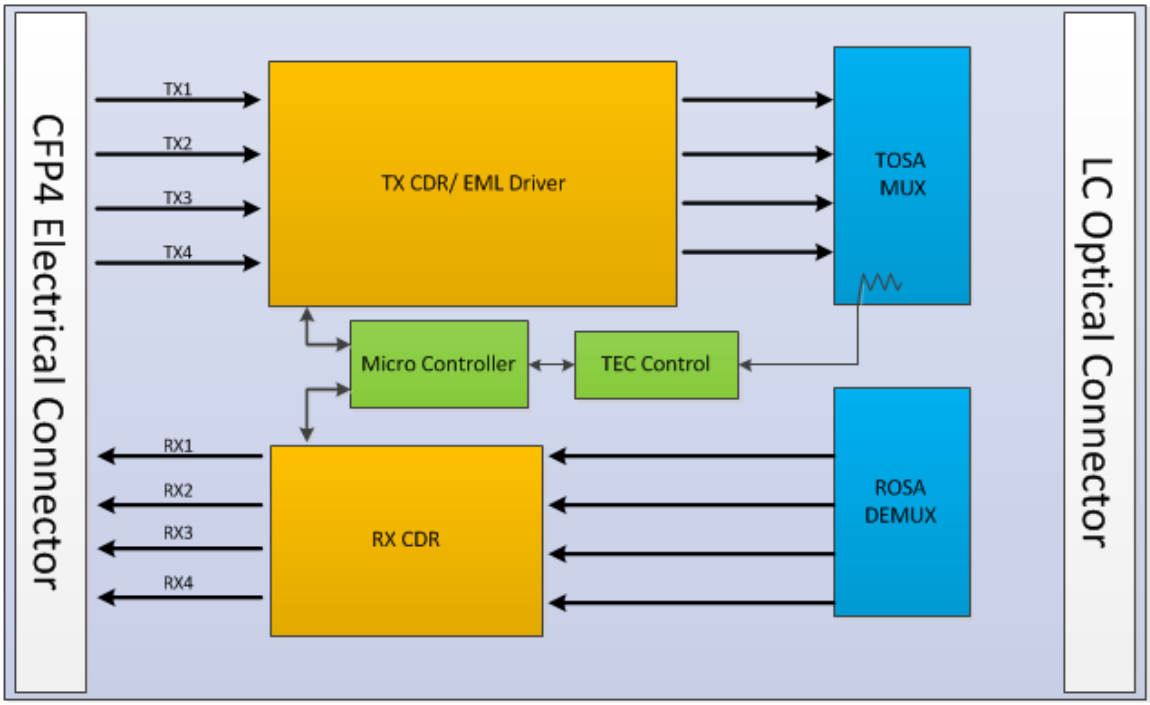

Figure 1. 100G CFP4 LR4 Transceiver Block Diagram

3. Pin Assignment and Description

The CFP4 electrical connector has 56 pins, which are arranged in top and bottom rows. The pin orientation is shown in Figure 2 and the pin map is shown in Table 2. The detailed description of the bottom side pins from pin 1 through pin 28 is shown in Table 3 while the description of the top side pins is shown in Table 4.

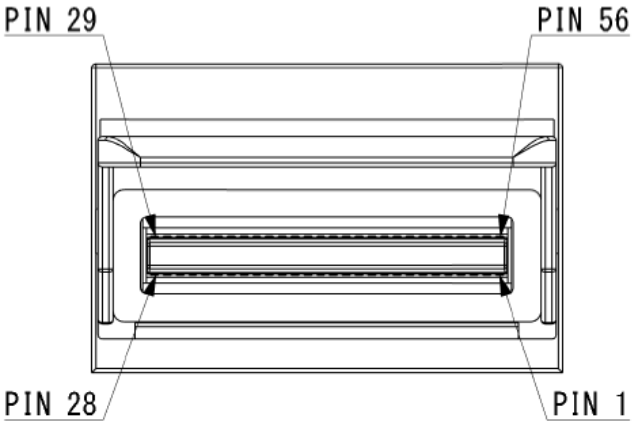

Figure 2. CFP4 Connector Pin Map Orientation

Table 2. Pin Map

	CFP4 Bottom		CFP4 Top	CFP4 Top ALT1
1	3.3V_GND	56	GND	GND
2	3.3V_GND	55	TX3n	TX0n
3	3.3V	54	TX3p	TX0p

Toward Host
(pin views from top)

4	3.3V	53	GND	GND
5	3.3V	52	TX2n	TX1n
6	3.3V	51	TX2p	TX1p
7	3.3V_GND	50	GND	GND
8	3.3V_GND	49	TX1n	TX2n
9	VND_IO_A	48	TX1p	TX2p
10	VND_IO_B	47	GND	GND
11	TX_DIS *(PRG_CNTL1)*	46	TX0n	TX3n
12	RX_LOS *(PRG_ALRM1)*	45	TX0p	TX3p
13	GLB_ALRMn	44	GND	GND
14	MOD_LOPWR	43	*(REFCLKn)*	*(REFCLKn)*
15	MOD_ABS	42	*(REFCLKp)*	*(REFCLKp)*
16	MOD_RSTn	41	GND	GND
17	MDC	40	RX3n	RX3p
18	MDIO	39	RX3p	RX3n
19	PRTADR0	38	GND	GND
20	PRTADR1	37	RX2n	RX2p
21	PRTADR2	36	RX2p	RX2n
22	VND_IO_C	35	GND	GND
23	VND_IO_D	34	RX1n	RX1p
24	VND_IO_E	33	RX1p	RX1n
25	GND	32	GND	GND
26	*(MCLKn)*	31	RX0n	RX0p
27	*(MCLKp)*	30	RX0p	RX0n
28	GND	29	GND	GND

REFCLK
(Optional)

MCLK = TX_MCLK + RX_MCLK
(Optional)

Table 3. Definition of the Bottom Side Pins from Pin 1 through Pin 28

PIN	Name	I/O	Logic	Description
1	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separated or tied together with Signal Ground
2	3.3V_GND			
3	3.3V			
4	3.3V			
5	3.3V			
6	3.3V			3.3V Module Supply Voltage
7	3.3V_GND			
8	3.3V_GND			
9	VIND_IO_A	I/O		Module Vendor I/O A. Do Not Connect
10	VIND_IO_B	I/O		Module Vendor I/O B. Do Not Connect

11	TX_DIS (PRG_CNTL1)	I	LVCMOS w/PUR	Transmitter Disable for all lanes. "1" or NC: Transmitter disabled; "0": transmitter enabled. (Optionally configurable as Programmable Control1 after Reset)
12	RX_LOS (PRG_ALRM1)	O	LVCMOS w/PUR	Receiver Loss of Optical Signal. "1": low optical signal; "0": normal condition (Optionally configurable as Programmable Alarm1 after Reset)
13	GLB_ALRMn	O	LVCMOS	Global Alarm. "0": alarm condition in any MDIO Alarm register; "1": no alarm condition, Open Drain, Pull up Resistor on Host
14	MOD_LOPWR	I	LVCMOS w/PUR	Module Low Power Mode. "1" or NC: module in low power (safe) mode; "0": power-on enabled
15	MOD_ABS	O	GND	Module Absent. "1" or NC: module absent; "0": module present, Pull up resistor on Host
16	MOD_RSTn	I	LVCMOS w/PDR	Module Reset. "0": resets the module; "1" or NC: module enabled, Pull down Resistor in Module
17	MDC	I	1.2V CMOS	Management Data Clock (electrical specs as per IEEE Std 802.3-2012)
18	MDIO	I/O	1.2V CMOS	Management Data I/O bi-directional data (electrical specs as per IEEE Std 802.3ae-2008 and ba-2010)
19	PRTADR0	I	1.2V CMOS	MDIO Physical Port address bit 0
20	PRTADR1	I	1.2V CMOS	MDIO Physical Port address bit 1
21	PRTADR2	I	1.2V CMOS	MDIO Physical Port address bit 2
22	VND_IO_C	I/O		Module Vendor I/O C. Do Not Connect
23	VND_IO_D	I/O		Module Vendor I/O D. Do Not Connect
24	VND_IO_E	I/O		Module Vendor I/O E. Do Not Connect
25	GND			
26	(MCLKn)	O	CML	For optical waveform testing. Not for normal use
27	(MCLKp)	O	CML	For optical waveform testing. Not for normal use
28	GND			

Table 4. Definition of Top Side Pins

PIN	Name		PIN	Name
29	GND		43	(REFCLKp)
30	RX0p		44	GND
31	RX0n		45	TX0p
32	GND		46	TX0n
33	RX1p		47	GND
34	RX1n		48	TX1p
35	GND		49	TX1n
36	RX2p		50	GND
37	RX2n		51	TX2p
38	GND		52	TX2n
39	RX3p		53	GND
40	RX3n		54	TX3p
41	GND		55	TX3n
42	(REFCLKn)		56	GND

4. Recommended Power Supply Filter

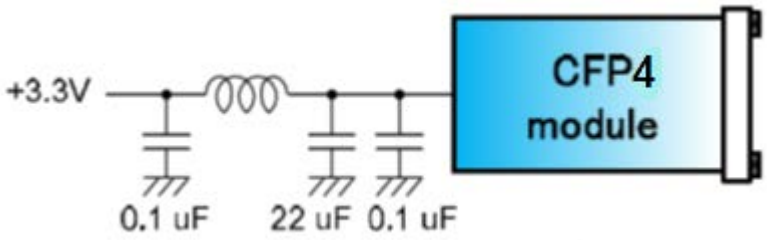

Figure 3. Recommended Power Supply Filter

5. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Storage Temperature	Ts	-40	85	degC	
Relative Humidity (non-condensation)	RH		85	%	
Operating Case Temperature	T_{OP}	0	70	degC	
Supply Voltage	Vcc	-0.5	3.6	V	
Voltage on LVTTL Input	Vilvttl	-0.5	VCC3+0.3	V	
LVTTL Output Current	Iolvttl		15	mA	
Voltage on Open Collector Output	Voco	0	6	V	
Damage Threshold, each Lane	TH_d	5.5		dBm	1

Notes:
1. PIN receiver.

6.Recommended Operating Conditions and Supply Requirements

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Operating Case Temperature	T_{OP}	0		70	degC	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Data Rate, each Lane			25.78125		Gbps	1
Data Rate, each Lane			27.9525		Gbps	2
Control Input Voltage High		2		Vcc	V	
Control Input Voltage Low		0		0.8	V	
Power Supply Noise	Vrip			2	%	DC-1MHz
				3	%	1-10MHz
Link Distance with G.652	D			10	km	

Notes:
1. 100GBASE-LR4.
2. OUT4 with FEC.

7. Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Power Consumption				6.0	W	

Supply Current	Icc			1820	mA	
Low Power Mode Power Dissipation				1.0	W	
Transmitter (each Lane)						
Single-ended Input Voltage Tolerance (Note 1)		-0.3		4.0	V	Referred to TP1 signal common
AC Common Mode Input Voltage Tolerance		15			mV	RMS
Differential Input Voltage Swing Threshold		50			mVpp	LOSA Threshold
Differential Input Voltage Swing	Vin,pp	190		700	mVpp	
Differential Input Impedance	Zin	90	100	110	Ohm	
Receiver (each Lane)						
Single-ended Output Voltage		-0.3		4.0	V	Referred to signal common
AC Common Mode Output Voltage				7.5	mV	RMS
Differential Output Voltage Swing	Vout,pp	300		850	mVpp	
Differential Output Impedance	Zout	90	100	110	Ohm	
Termination Mismatch at 1MHz				5	%	

Notes:

1. The single ended input voltage tolerance is the allowable range of the instantaneous input signals.

8. Optical Characteristics

CFP4 100GBASE-LR4 & OTU4						
Parameter	**Symbol**	**Min**	**Typical**	**Max**	**Unit**	**Notes**
Lane Wavelength	L0	1294.53	1295.56	1296.59	nm	
	L1	1299.02	1300.05	1301.09	nm	
	L2	1303.54	1304.58	1305.63	nm	
	L3	1308.09	1309.14	1310.19	nm	
Transmitter						
SMSR	SMSR	30			dB	
Total Average Launch Power	P_T			10.5	dBm	
Average Launch Power, each Lane	P_{AVG}	-4.3		4.5	dBm	
OMA, each Lane	P_{OMA}	-1.3		4.5	dBm	1
Difference in Launch Power between any Two Lanes (OMA)	Ptx,diff			5	dB	
Launch Power in OMA minus Transmitter and Dispersion Penalty (TDP), each Lane		-2.3			dBm	2

TDP, each Lane	TDP			2.2	dB	2
Extinction Ratio	ER	4			dB	
$RIN_{20}OMA$	RIN			-130	dB/Hz	
Optical Return Loss Tolerance	TOL			20	dB	
Transmitter Reflectance	R_T			-12	dB	
Eye Mask{X1, X2, X3, Y1, Y2, Y3}		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}				3
Average Launch Power OFF Transmitter, each Lane	Poff			-30	dBm	
Receiver						
Damage Threshold, each Lane	TH_d	5.5			dBm	
Total Average Receive Power				10.5	dBm	
Average Receive Power, each Lane		-10.6		4.5	dBm	
Receive Power (OMA), each Lane				4.5	dBm	
Receiver Sensitivity (OMA), each Lane	SEN			-8.6	dBm	2
Stressed Receiver Sensitivity (OMA), each Lane				-6.8	dBm	2, 4
Difference in Receive Power between any Two Lanes (OMA)	Prx,diff			5.5	dB	
LOS Assert	LOSA		-18		dBm	
LOS Deassert	LOSD		-15		dBm	
LOS Hysteresis	LOSH	0.5			dB	
Receiver Electrical 3 dB upper Cutoff Frequency, each Lane	Fc			31	GHz	
Conditions of Stress Receiver Sensitivity Test (Note 5)						
Vertical Eye Closure Penalty, each Lane			1.8		dB	
Stressed Eye J2 Jitter, each Lane			0.3		UI	
Stressed Eye J9 Jitter, each Lane			0.47		UI	

Notes:
1. Even if TDP < 1 dB, the OMA min must exceed the minimum value specified here.
2. Only for 100GBASE-LR4.
3.See Figure 4 below.
4.Measured with conformance test signal at receiver input for BER = $1x10^{-12}$.
5.Vertical eye closure penalty, stressed eye J2 Jitter, and stressed eye J9 Jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

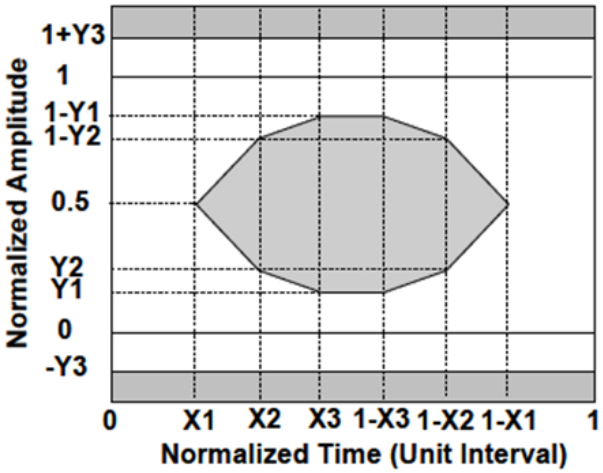

Figure 4. Eye Mask Definition

9. Mechanical Dimensions

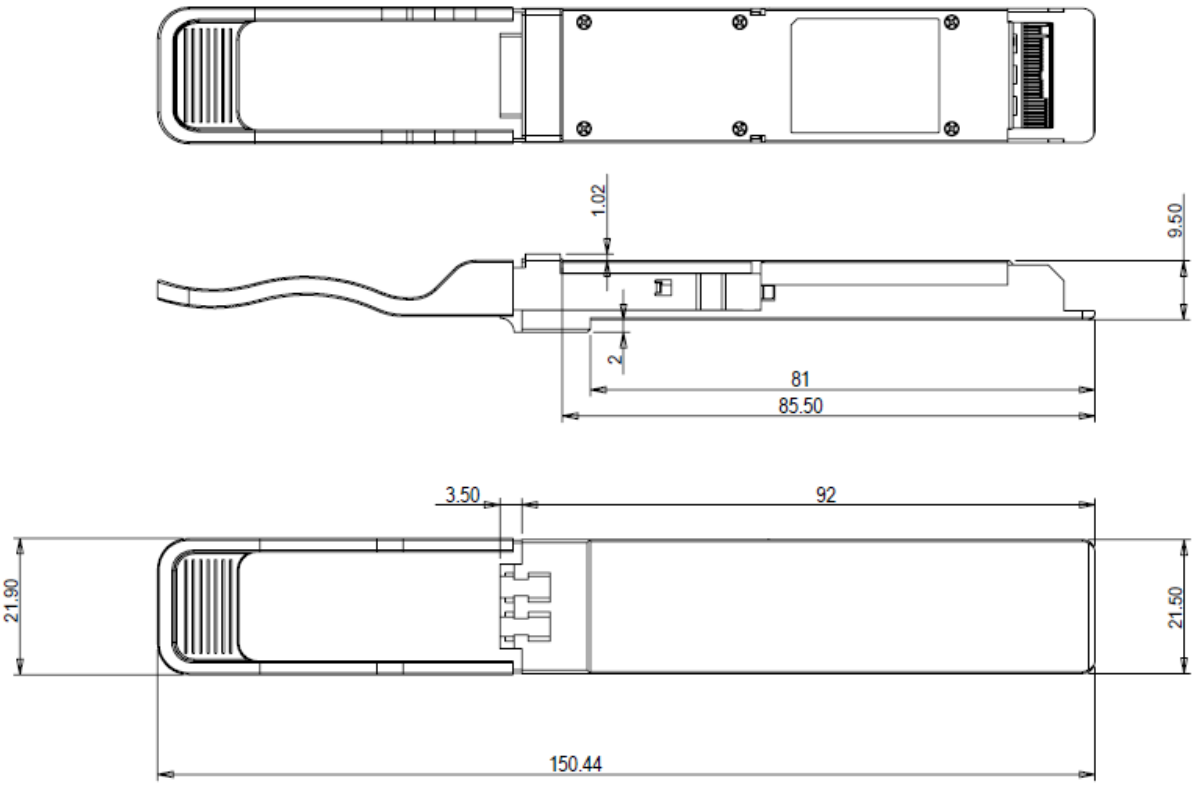

Figure 5. Mechanical Outline

10.ESD

This transceiver is specified as ESD threshold 2kV for all electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

11. Laser Safety

This is a Class 1 Laser Product according to IEC 60825-1:1993:+A1:1997+A2:2001. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (July 26, 2001)