Features:

- ✧ Hot-pluggable CFP2 form factor
- ✧ Supports 103.1Gb/s and 112Gb/s aggregate bit rates
- ✧ Power dissipation < 4W
- ✧ RoHS-6 compliant (lead-free)
- ✧ Commercial case temperature range of 0°C to 70°C
- ✧ Single 3.3V power supply
- ✧ Maximum link length of 100m on OM3 Multimode Fiber (MMF) and 150m on OM4 MMF
- ✧ Uncooled 10x10Gb/s 850nm transmitter
- ✧ CPPI electrical interface
- ✧ Single MPO24 receptacle
- ✧ MDIO management interface
- ✧ Tx/Rx optical power monitoring functionality

Applications:

- ✧ 100GBASE-SR10 Ethernet
- ✧ 10x11.2Gb/s Multimode OTN
- ✧ 2x 40GBASE-SR4 Ethernet
- ✧ 10x 10GE-SR Lite Ethernet

Description:

OPWAY's OPC2E01 100G CFP2 transceiver modules are designed for use in 100 Gigabit Ethernet links and 10x11.2G OTN client interfaces over multimode fiber. They are compliant with the CFP2 MSA[1] and with IEEE 802.3ba 100GBASE-SR10[2]. The transceiver is RoHS-6 compliant and lead-free per Directive 2002/95/EC[3].

● Absolute Maximum Ratings

Module performance is not guaranteed beyond the operating range (see **Environmental Specifications** Section). Exceeding the limits below may damage the transceiver module permanently.

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Maximum Supply Voltage	Vcc	-0.5		4.0	V	
Storage Temperature	TS	-40		85	□C	
Case Operating Temperature	TOP	0		70	□C	
Relative Humidity	RH	15		85	%	1
Receiver Damage Threshold, per Lane	PRdmg	5.5			dBm	

Notes:

1. Non-condensing.

● Electrical Characteristics (EOL, T_{OP} = 0 to 70℃, V_{CC} = 3.13 to 3.47 Volts)

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Supply Voltage	Vc	3.13		3.47	V	
Supply Current	Icc			TBD	mA	
Module Total Power	P			4.0	W	1
Transmitter (per Lane)						
Signaling rate per lane		10.3125		11.181	Gb/s	2

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Single ended input voltage tolerance	VinT	-0.3		4.0	V	
Differential data input swing	Vin,pp	120		1200	mVpp	3
Differential input threshold			50		mV	
AC common mode input voltage tolerance (RMS)		15			mV	
Differential input return loss		Per IEEE 802.3ba, Section 86A.4.1.1			dB	4
J2 Jitter Tolerance	Jt2	0.17			UI	
J9 Jitter Tolerance	Jt9	0.29			UI	
Data Dependent Pulse Width Shrinkage	DDPWS	0.07			UI	
Eye mask coordinates {X1, X2, Y1, Y2}		0.11, 0.31, 95, 350			UI mV	5
Receiver (per Lane)						
Signaling rate per lane		10.3125		11.1810	Gb/s	2
Single-ended output voltage		-0.3		4.0	V	
Differential data output swing	Vout,pp	300		800	mVpp	6
AC common mode output voltage (RMS)				7.5	mV	
Termination mismatch at 1 MHx				5	%	
Differential output return loss		Per IEEE 802.3ba, Section 86A.4.2.1			dB	4
Common mode output return loss		Per IEEE 802.3ba, Section 86A.4.2.2			dB	4
Output transition time, 20% to 80%		28			ps	
J2 Jitter output	Jo2			0.42	UI	
J9 Jitter output	Jo9			0.65	UI	
Eye mask coordinates {X1, X2 Y1, Y2}		0.29, 0.5 150, 425			UI mV	5
Power Supply Ripple Tolerance	PSR	Per CFP MSA1			mVpp	

Notes:

1. Maximum total power value is specified across the full temperature and voltage range.
2. +/- 100ppm at 10.3125 Gb/s and +/-20ppm at 11.1810 Gb/s.
3. After internal AC coupling. Self-biasing 100□ differential input.
4. 10 MHz to 11.1 GHz range
5. Hit ratio = 5 x 10E-5
6. AC coupled with 100Ω differential output impedance. Limiting output.

OPC2E01 Clocking Signals

Clock Name	Status	I/O	Value
REFCLK	Not Required	I	Not required; terminated internally.

- **Optical Characteristics (EOL, T_{OP} = 0 to 70℃, V_{CC} = 3.13 to 3.47 Volts)**

Parameter	Symbol	Min	Typ	Max	Unit	Ref
Transmitter (per Lane)						
Signaling Speed per Lane		10.3125		11.1810	GBd	1
Center wavelength		840		860	nm	
RMS Spectral Width	SW			0.65	nm	
Average Launch Power per Lane	TXP_X	-7.6		2.4	dBm	
Transmit OMA per Lane	TxOMA	-5.6		3.0	dBm	2
Difference in Power between any two lanes [OMA]	DP_X			4.0	dB	
Peak Power per Lane	PP_X			4.0	dBm	
Launch Power [OMA] minus TDP per Lane	P-TDP	-6.5			dBm	
TDP per Lane	TDP			3.5	dBm	
Optical Extinction Ratio	ER	3.0			dB	
Optical Return Loss Tolerance	ORL			12	dB	
Encircled Flux	FLX	> 86% at 19 um < 30% at 4.5 um			dBm	
Average launch power of OFF transmitter, per lane				-30	dBm	
Relative Intensity Noise	RIN			-128	dB/Hz	3
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}		0.23, 0.34, 0.43, 0.27, 0.35, 0.4				
Receiver (per Lane)						
Signaling Speed per Lane		10.3125		11.1810	GBd	4
Center wavelength		840		860	nm	
Average Receive Power per Lane	RXP_X	-9.5		2.4	dBm	
Receive Power (OMA) per Lane	RxOMA			3	dBm	
Stressed Receiver Sensitivity (OMA) per Lane	SRS			-5.4	dBm	
Back to Back Receiver Sensitivity (OMA) per Lane	RxSens			-8.7	dBm	5
Peak Power, per lane	PP_X			4	dBm	
Receiver Reflectance	Rfl			-12	dB	
Vertical eye closure penalty, per lane				1.9	dB	
Stressed eye J2 jitter, per Lane				0.3	UI	
Stressed eye J9 jitter, per Lane				0.47	UI	
OMA of each aggressor lane				-0.4	dBm	
Receiver jitter tolerance [OMA], per Lane				-5.4	dBm	
Rx jitter tolerance: Jitter frequency and p-p amplitude		(75, 5)			kHz, UI	
		(375, 1)			kHz, UI	
LOS De-Assert	LOS_D			-11	dBm	
LOS Assert	LOS_A	-30		-14	dBm	
LOS Hysteresis		0.5			dB	

Notes:

1. Transmitter consists of 10 lasers operating at a maximum rate of 11.1810 Gb/s each.

2. Even if TDP is <0.9dB, the OMA min must exceed this value.
3. RIN is scaled by 10*log (10/4) to maintain SNR outside of transmitter.
4. Receiver consists of 10 photodetectors operating at a maximum rate of 11.1810 Gb/s each.
5. Measured using DUT Tx and DUT Rx; no golden transmitters shall be used.

● General Specifications

Parameter		Symbol	Min	Typ	Max	Units	Ref.
Bit Rate (all lanes combined)		BR	103.1		112.0	Gb/s	1
Bit Error Ratio		BER			10^{-12}		2
Maximum Supported Distances							
Fiber Type							
OM3 MMF		Lmax1			100	m	
OM4 MMF		Lmax2			150	m	

Notes:
1. Supports 100GBASE-SR10 per IEEE 802.3ba and 10x11.2 multimode OTN.
2. Tested with a 231-1 PRBS

● Environmental Specifications

OPWAY OPC2E01 CFP2 transceivers have an operating case temperature range of 0°C to +70°C.

Parameter	Symbol	Min	Typ	Max	Units	Ref.
Case Operating Temperature	T_{op}	0		70	°C	
Storage Temperature	T_{sto}	-40		85	°C	

● Regulatory Compliance

OPWAY OPC2E01 CFP2 transceivers are Class 1 laser eye safety compliant per IEC 60825-1. They are certified per the following standards:

Feature	Agency	Standard	Certificate Number
Laser Eye Safety	FDA/CDRH	CDRH 21 CFR 1040 and Laser Notice 50	9210176
Laser Eye Safety	TÜV	EN 60950-1: 2006+A11 EN 60825-1: 2007 EN 60825-2: 2004+A1+A2	TBD
Electrical Safety	TÜV	EN 60950	TBD
Electrical Safety	UL/CSA	CLASS 3862.13 CLASS 3862.93	TBD

● Digital Diagnostics Functions

OPC2E01 CFP2 transceivers support the MDIO-based diagnostics interface specified in the CFP MSA Management Interface Specification, Rev 2.2[1].

● Memory Contents

Per the CFP MSA[1].

● Host PCB Layout and Bezel Recommendations

Per CFP2 Hardware Specification[1].

● Mechanical Specifications

OPWAY OPC2E01 CFP2 transceivers are compatible with the CFP2 Hardware Specification for pluggable form factor modules.

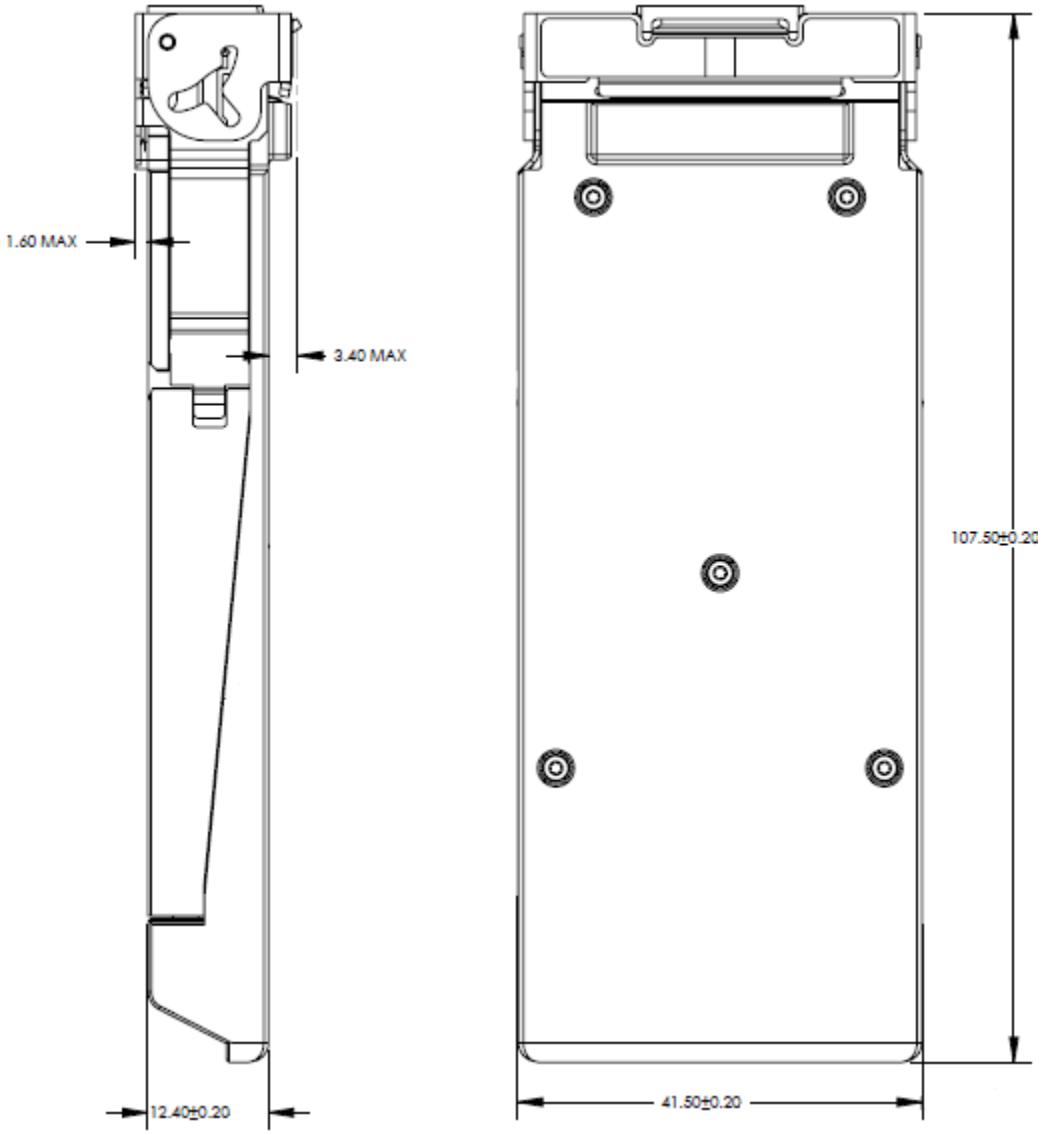


Figure 1. Mechanical Dimensions

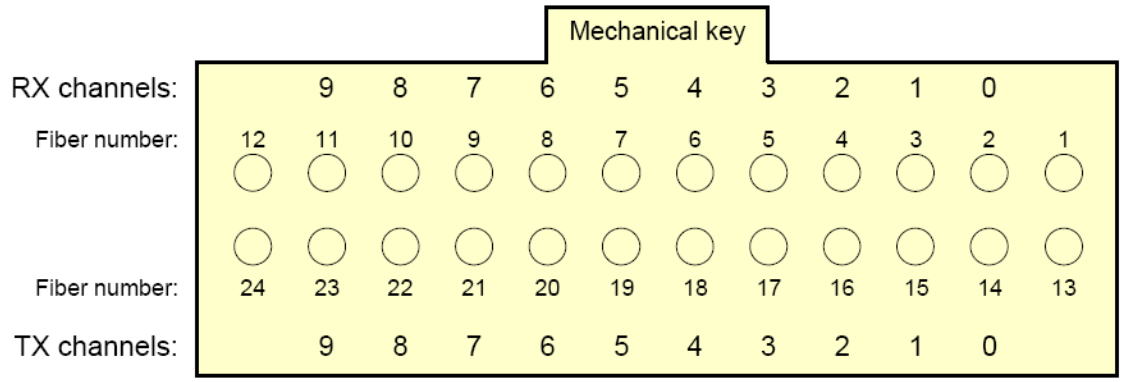


Figure 2. Optical Lane Assignment
(View from the front, looking into the MPO receptacle)

● Pin Layout

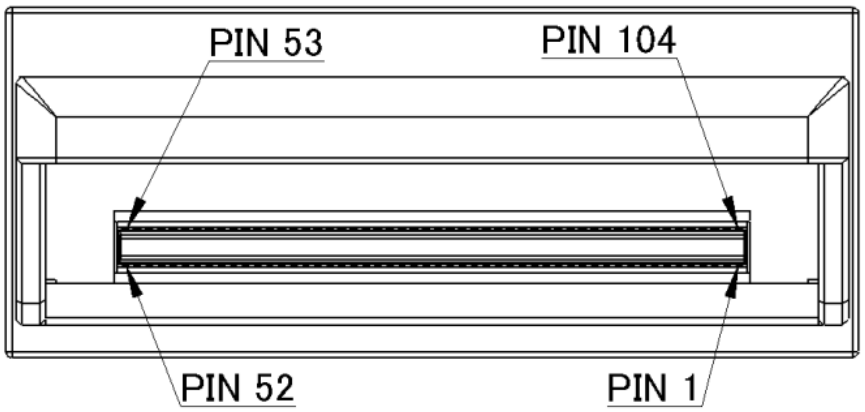
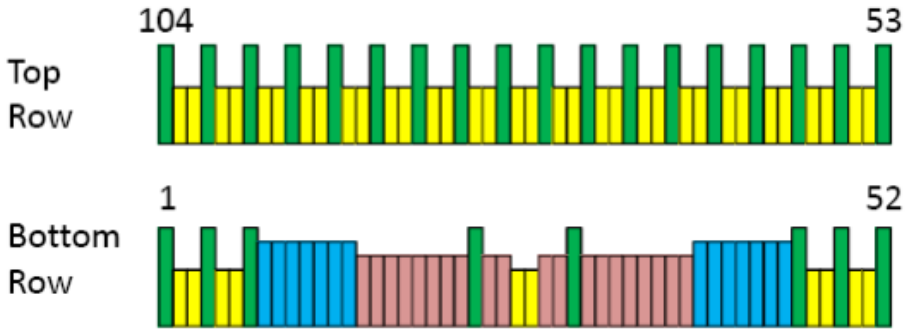
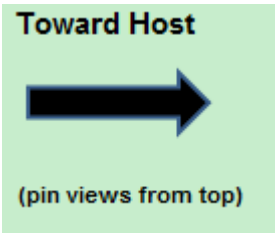


Figure 3. CFP2 Module Pad Layout



	CFP2 Bottom
1	GND
2	TX9n
3	TX9p
4	GND
5	TX8n
6	TX8p
7	3.3V_GND

	CFP2 Top
104	GND
103	TX7n
102	TX7p
101	GND
100	TX6n
99	TX6p
98	GND



8	3.3V_GND	97	TX5n
9	3.3V	96	TX5p
10	3.3V	95	GND
11	3.3V	94	TX4n
12	3.3V	93	TX4p
13	3.3V_GND	92	GND
14	3.3V_GND	91	TX3n
15	VND_IO_A	90	TX3p
16	VND_IO_B	89	GND
17	PRG_CNTL1	88	TX2n
18	PRG_CNTL2	87	TX2p
19	PRG_CNTL3	86	GND
20	PRG_ALRM1	85	TX1n
21	PRG_ALRM2	84	TX1p
22	PRG_ALRM3	83	GND
23	GND	82	TX0n
24	TX_DIS	81	TX0p
25	RX_LOS	80	GND
26	MOD_LOPWR	79	*(REFCLKn)*
27	MOD_ABS	78	*(REFCLKp)*
28	MOD_RSTn	77	GND
29	GLB_ALRMn	76	RX7n
30	GND	75	RX7p
31	MDC	74	GND
32	MDIO	73	RX6n
33	PRTADR0	72	RX6p
34	PRTADR1	71	GND
35	PRTADR2	70	RX5n
36	VND_IO_C	69	RX5p
37	VND_IO_D	68	GND
38	VND_IO_E	67	RX4n
39	3.3V_GND	66	RX4p
40	3.3V_GND	65	GND
41	3.3V	64	RX3n
42	3.3V	63	RX3p
43	3.3V	62	GND
44	3.3V	61	RX2n
45	3.3V_GND	60	RX2p
46	GND	59	GND
47	RX9n	58	RX1n
48	RX9p	57	RX1p
49	GND	56	GND
50	RX8n	55	RX0n
51	RX8p	54	RX0p
52	GND	53	GND

REFCLK
(Optional)

Figure 4. CFP2 Module Pin Map

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Note1:Pin 15,16,36,37,38, are internally used and NOT allowed to connect any signal and power supply or GND
Note2: Pin 2,3,50,51 are disabled unless MCLK output is enabled via MDIO

Pin Definition

Table 12 100Gb/s CFP2 Pin Definition(Bottom raw)

PIN	Name	I/O	Logic	Description
1	GND			
2	TX9n	I		Lane #9 Transmitter pin (+)
3	TX9p	I		Lane #9 Transmitter pin (-)
4	GND			
5	TX8n	I		Lane #8 Transmitter pin (+)
6	TX8p	I		Lane #8 Transmitter pin (-)
7	GND			
8	3.3V_GND			**3.3V Module Supply Voltage Return Ground, internally connected to Signal Ground**
9	3.3V			3.3V Module Supply Voltage
10	3.3V			
11	3.3V			
12	3.3V			
13	3.3V_GND			**3.3V Module Supply Voltage Return Ground, internally connected to Signal Ground**
14	3.3V_GND			
15	VND_IO_A	I/O		Module Vendor I/O A. Do Not Connect!
16	VND_IO_B	I/O		Module Vendor I/O B. Do Not Connect!
17	PRG_CNTL1	I	LVCMOS w/ PUR	Programmable Control 1 set over MDIO
18	PRG_CNTL2	I	LVCMOS w/ PUR	Programmable Control 2 set over MDIO
19	PRG_CNTL3	I	LVCMOS w/ PUR	Programmable Control 3 set over MDIO
20	PRG_ALRM1	O	LVCMOS	Programmable Alarm 1 set over MDIO
21	PRG_ALRM2	O	LVCMOS	Programmable Alarm 2 set over MDIO
22	PRG_ALRM3	O	LVCMOS	Programmable Alarm 3 set over MDIO
23	GND			
24	TX_DIS	I	LVCMOS w/ PUR	Transmitter Disable for all lanes, "1" or NC = transmitter disabled, "0" = transmitter enabled
25	RX_LOS	O	LVCMOS	Receiver Loss of Optical Signal, "1": low optical signal, "0":
26	MOD_LOPWR	I	LVCMOS w/ PUR	Module Low Power Mode. "1" or NC: module in low power (safe) mode, "0": power-on enabled
27	MOD_ABS	O	GND	Module Absent. "1" or NC: module absent, "0": module present, Pull Up Resistor on Host
28	MOD_RSTn	I	LVCMOS w/ PDR	Module Reset. "0" resets the module, "1" or NC = module enabled, Pull Down Resistor in Module
29	GLB_ALRMn	O	LVCMOS	Global Alarm. "0": alarm condition in any MDIO Alarm register, "1": no alarm condition, Open Drain, Pull Up Resistor on Host

30	GND			
31	MDC	I/O	1.2V CMOS	Management Data I/O bi-directional data (electrical specs as per
32	MDIO	I	1.2V CMOS	Management Data Clock (electrical specs as per 802.3ae and ba)
33	PRTADR0	I	1.2V CMOS	MDIO Physical Port address bit 0
34	PRTADR1	I	1.2V CMOS	MDIO Physical Port address bit 1
35	PRTADR2	I	1.2V CMOS	MDIO Physical Port address bit 2
36	VND_IO_C	I/O		Module Vendor I/O C. Do Not Connect!
37	VND_IO_D	I/O		Module Vendor I/O D. Do Not Connect!
38	VND_IO_E	I/O		Module Vendor I/O E. Do Not Connect!
39	3.3V_GND			**3.3V Module Supply Voltage Return Ground, internally connected to Signal Ground**
40	3.3V_GND			
41	3.3V			3.3V Module Supply Voltage
42	3.3V			
43	3.3V			
44	3.3V			
45	3.3V_GND			**3.3V Module Supply Voltage Return Ground, internally connected to Signal Ground**
46	GND			
47	RX9n	O		Lane #9 Receiver pin (+)
48	RX9p	O		Lane #9 Receiver pin (-)
49	GND			
50	RX8n	O		Lane #8 Receiver pin (+)
51	RX8p	O		Lane #8 Receiver pin (-)
52	GND			

● Management Interface

OPWAY OPC2E01 CFP transceivers support the MDIO interface specified in IEEE802.3 Clause 45. This 2-wire management data I/O interface is provided for the module status monitoring and control. The management data clock (MDC) provides clocking for the data that is passed on the MDIO port. Five further pins allow for loading of a port address (PORT_ADDR0-4) into the module.

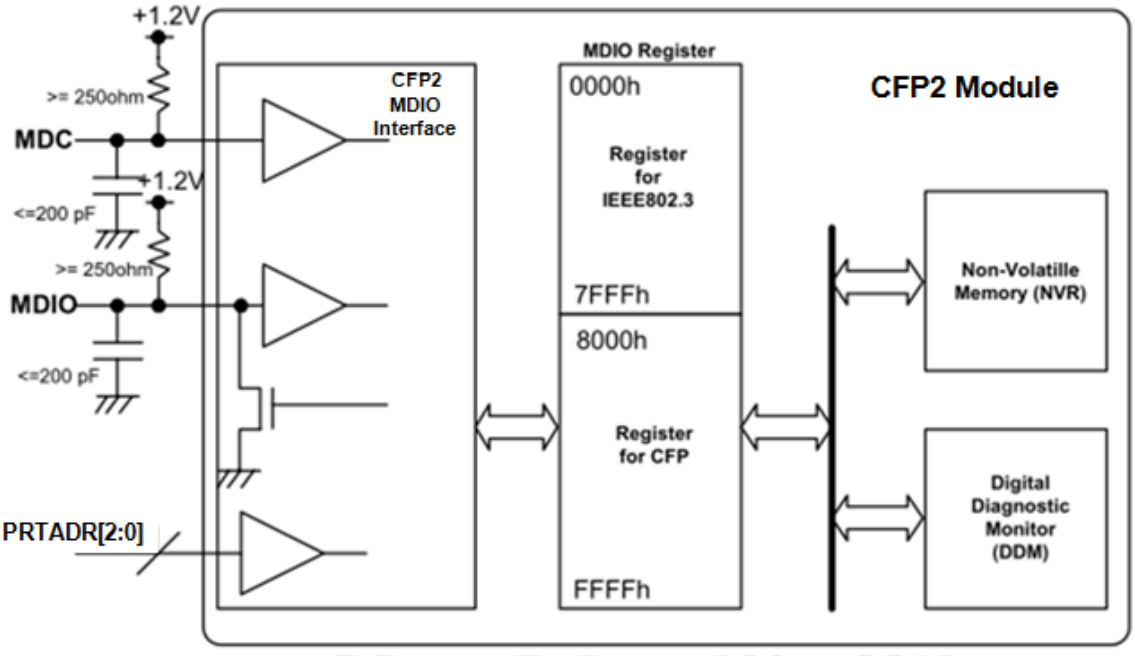

Figure 5. CFP MDIO Interface

Note: Capacitor represents stray capacity 600ohm pull-up is preferred

For more detailed information please refer to "***CFP MSA Management Interface Specification Version 2.2 r06***".

● Warnings

Handling Precautions: This device is susceptible damaged as a result of electrostatic discharge (ESD). A static free environment is highly recommended. Follow guidelines according to proper ESD procedures.

Laser Safety: Radiation emitted by laser devices can be dangerous to human eyes. Avoid eye exposure to direct or indirect radiation.

I. References

1. CFP2 Hardware Specification and CFP MSA Management Interface Specifications (MIS), Rev 2.2; CFP MSA, www.cfp-msa.org
2. IEEE 802.3ba, PMD Type 100GBASE-SR10.
3. Directive 2002/95/EC of the European Council Parliament and of the Council, "on the restriction of the use of certain hazardous substances in electrical and electronic equipment". January 27, 2003.