

# 10G XFP BIDI Optical Transceiver PN: OPP920-3327 Product Specification

#### **Features:**

- ♦ Supports 9.95Gb/s to 11.3Gb/s bit rates
- ♦ Hot pluggable 30 pin connector
- ♦ Compliant with XFP MSA
- ♦ Single LC for Bi-directional Transmission
- ♦ Transmission distance of 20km over Single mode fiber
- ♦ Uncooled 1330nm DFB Laser
- ♦ 2-wire interface for management and diagnostic monitor
- ♦ Single power supply voltages : +3.3V

- ♦ Temperature range  $0^{\circ}$ C to  $70^{\circ}$ C
- $\diamond$  Power dissipation < 1.5W
- ♦ RoHS Compliant

## **Applications:**

- ♦ 10GBASE-LR/LW Ethernet
- ♦ SONET OC-192 /SDH STM-64
- ♦ 1200-SM-LL-L 10G Fibre Channel

### **Description:**

OPWAY' OPP920-3327 Small Form Factor 10Gb/s (XFP) transceivers are compliant with the current XFP Multi-Source Agreement (MSA) Specification. The high performance uncooled 1330nm DFB transmitter and high sensitivity PIN receiver provide superior performance for Multiple applications up to 20km links.



## • Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	
Storage Temperature	$T_{ST}$	-40	+85	°C	
Case Operating Temperature	Тс	0	+70	°C	
Supply Voltage	V <sub>CC</sub>	-0.5	+4.0	V	

## • Electrical Characteristics

Parameter	Symbol	Min	Тур	Max	Unit	Note
Supply Voltage	Vcc	3.13		3.45	V	
Supply Current	Icc			455	mA	
Module total power	Р			1.5	W	
Transmitter						
Input differential impedance	Rin		100		Ω	1
Differential data input swing	Vin,pp	100		1000	mV	
Transmit Disable Voltage	VD	2.0		Vcc	V	
Transmit Enable Voltage	V <sub>EN</sub>	GND		GND+0.8	V	
Receiver						
Differential data output swing	Vout,pp	120		800	mV	
LOS Fault	VLOS fault	Vcc – 0.5		Vcc <sub>HOST</sub>	V	2
LOS Normal	VLOS norm	GND		GND+0.5	V	2

Notes

1. Connected directly to TX data input pins. AC coupling from pins into laser driver IC.

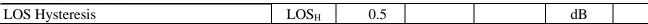
2. LOS is an open collector output. Should be pulled up with  $4.7k - 10k\Omega$  on the host board. Normal operation is logic 0; loss of signal is logic 1.

## • Optical Characteristics

Parameter	Symbol	Min	Тур	Max	Unit	Ref.
Transmitter						
Operating Date Rate	BR	9.95		11.3	Gb/s	
Optical Wavelength	λ	1320	1330	1340	nm	
RMS Spectral Width	$\lambda_{RMS}$			1	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Launch Power	Pout	-2		+3	dBm	
Average Launch power of OFF Transmitter	P <sub>OFF</sub>			-30	dBm	
Optical Extinction Ratio	ER	3.5			dB	
Receiver						
Operating Date Rate	BR	9.95		11.3	Gb/s	
Optical Center Wavelength	$\lambda_{\rm C}$	1260	1270	1280	nm	
Receiver Sensitivity	Sen			-14.5	dBm	1
Input Saturation Power(Overload)	Sat	0			dBm	
LOS Assert	LOSA	-30			dBm	
LOS De-Assert	LOS <sub>D</sub>			-15	dBm	

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#### Notes:

1. Measured with a PRBS  $2^{31}$  -1 test pattern, @10.3125Gb/s, BER <  $10^{-12}$ .

## • Pin Assignment

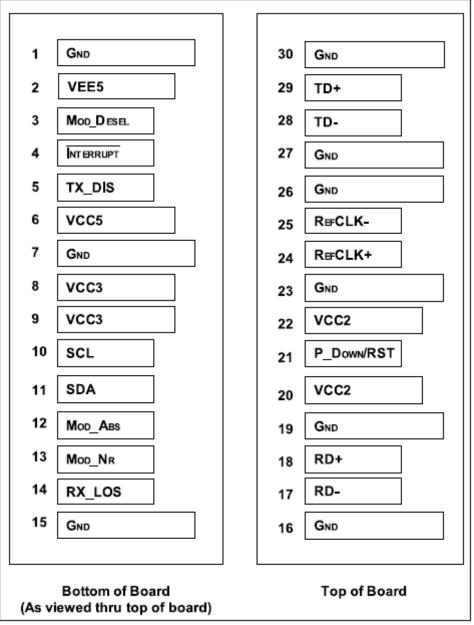


Diagram of Host Board Connector Block Pin Numbers and Names

### • Pin Function Definitions

Pin	Logic	Symbol	Name/Description	
1		GND	Module Ground	1
2		VEE5	Optional –5.2 Power Supply – Not required	
3	LVTTL-I	Mod-Desel	Module De-select; When held low allows the module to respond to 2-wire serial interface	
4	LVTTL-O	Interrupt	Interrupt (bar); Indicates presence of an important condition which can be read over the serial 2-wire interface	2
5	LVTTL-I	TX_DIS	Transmitter Disable; Turns off transmitter laser output	

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6		VCC5	+5 Power Supply	
7		GND	Module Ground	1
8		VCC3	+3.3V Power Supply	
9		VCC3	+3.3V Power Supply	
10	LVTTL- I/O	SCL	2-Wire Serial Interface Clock	2
11	LVTTL- I/O	SDA	2-Wire Serial Interface Data Line	
12	LVTTL-O	Mod_Abs	Indicates Module is not present. Grounded in the Module	2
13	LVTTL-O	Mod_NR	Module Not Ready; Indicating Module Operational Fault	2
14	LVTTL-O	RX_LOS	Receiver Loss of Signal indicator	2
15		GND	Module Ground	1
16		GND	Module Ground	1
17	CML-O	RD-	Receiver inverted data output	
18	CML-O	RD+	Receiver non-inverted data output	
19		GND	Module Ground	
20		VCC2	+1.8V Power Supply – Not required	
21	LVTTL-I	P_Down/RST	Power down; When high, requires the module to limit power consumption to 1.5W or below. 2-Wire serial interface must be functional in the low power mode. Reset; The falling edge initiates a complete reset of the module	
			including the 2-wire serial interface, equivalent to a power cycle.	
22		VCC2	+1.8V Power Supply – Not required	
23		GND	Module Ground	1
24	PECL-I	RefCLK+	Reference Clock non-inverted input, AC coupled on the host board – Not required	
25	PECL-I	RefCLK-	Reference Clock inverted input, AC coupled on the host board – Not required	
26		GND	Module Ground	
27		GND	Module Ground	
28	CML-I	TD-	Transmitter inverted data input	
29	CML-I	TD+	Transmitter non-inverted data input	
30		GND	Module Ground	1
Note				

#### Note

1. Module circuit ground is isolated from module chassis ground within the module.

2. Open collector; should be pulled up with 4.7k - 10k ohms on host board to a voltage between 3.15Vand 3.45V. 3. A Reference Clock input is not required.

#### • Digital Diagnostic Functions

As defined by the XFP MSA, OPWAY's XFP transceivers provide digital diagnostic functions via a 2-wire serial interface, which allows real-time access to the following operating parameters:

- ✓ Transceiver temperature
- ✓ Laser bias current
- ✓ Transmitted optical power
- ✓ Received optical power
- ✓ Transceiver supply voltage

It also provides a sophisticated system of alarm and warning flags, which may be used to alert end-users when particular operating parameters are outside of a factory-set normal range.

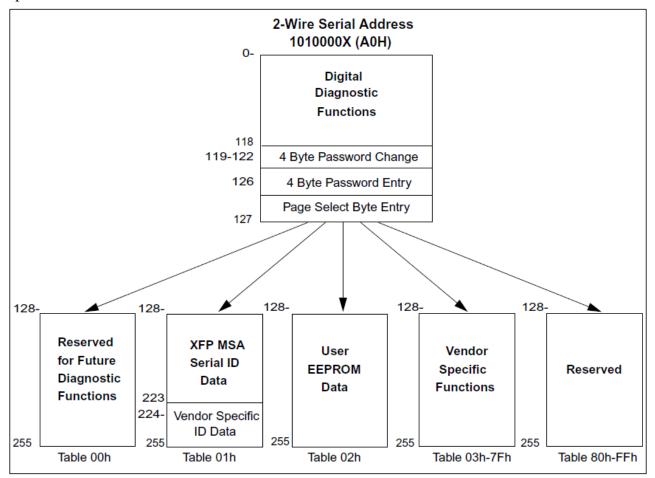
The operating and diagnostics information is monitored and reported by a Digital Diagnostics Transceiver Controller (DDTC) inside the transceiver, which is accessed through the 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL pin) is generated by the

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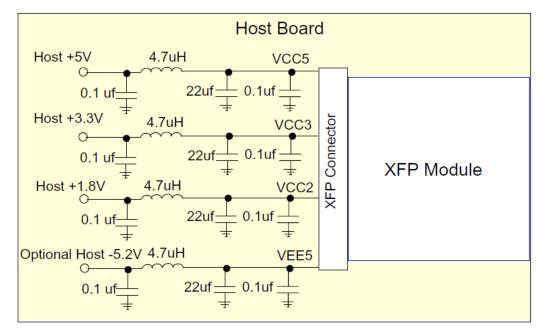
host. The positive edge clocks data into the XFP transceiver into those segments of its memory map that are not write-protected. The negative edge clocks data from the XFP transceiver. The serial data signal (SDA pin) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially. The 2-wire serial interface provides sequential or random access to the 8 bit parameters, addressed from 000h to the maximum address of the memory.

For more detailed information including memory map definitions, please see the XFP MSA Specification.

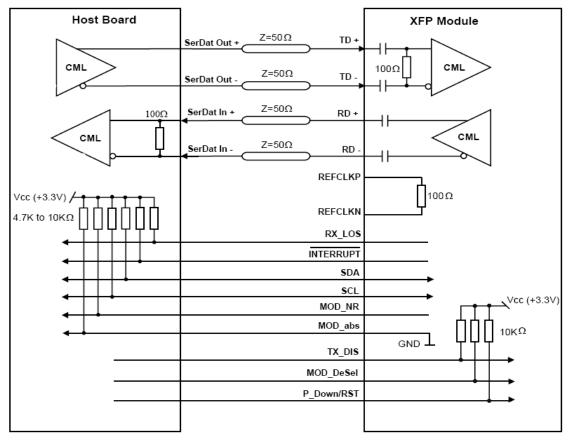




### • Recommended Circuit



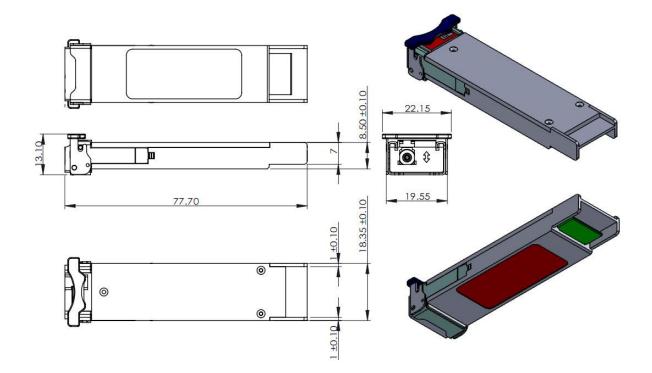
**Recommended Host Board Power Supply Circuit** 



**Recommended High-speed Interface Circuit** 



## • Mechanical Dimensions(Unit:mm)



## • Document Revision

Version No.	Date	Reviser	Description
V1.0	2023-11-16	Kevin	Template update

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